

SEMICONDUCTOR DEVICE CONDUCTIVE BUMP AND INTERCONNECT BARRIER

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Inventor(s): BRAECKELMANN GREGOR (US); VENKATESAN SURESH (US); VENKATRAMAN RAMNATH (US); CLEGG DAVID B (US); ANTHONY BRIAN G (US); COLE REBECCA G (US); CROWN STEPHEN R (US); GREER STUART E (US); REBER DOUGLAS M (US); ADETUTU OLUBUNMI (US); BARR ALEXANDER L (US)

Applicant(s):

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Abstract

An interconnect overlies a semiconductor device substrate (10). In one embodiment, a conductive barrier layer overlies a portion of the interconnect, a passivation layer (92) overlies the conductive barrier layer and the passivation layer (92) has an opening that exposes portions of the conductive barrier layer (82). In an alternate embodiment a passivation layer (22) overlies the interconnect, the passivation layer (22) has an opening (24) that exposes the interconnect and a conductive barrier layer (32) overlies the interconnect within the opening (24)

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